**Date:**

**Ahsanullah University of Science and Technology**

Department of Computer Science and Engineering

Third Year, First Semester Clearance/ Improvement/ Carry Over Examination, Fall 2016

Course No: **CSE 3109** Course Title: **Digital System Design**

Time: 3 Hours Full Marks: 70

**[ There are 7(Seven) questions. Answer any 5(Five) questions.]**

**[*Marks allotted are indicated in the right margin within ‘[ ]’.*]**

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| --- | --- | --- |
| 1.a) | What is Shift Register? | [2] |
| b) | Design a 4-bit binary counter by using J-K flip flops. | [3] |
| c) | A combinational circuit is defined by the functions:  F1(A,B,C) = ∑ (3, 5, 6, 7)  F2(A,B,C) = ∑ (0, 2, 4, 7)  Implement the circuit with a PLA having three inputs, four product terms, and two outputs. | [4] |
| d) | The inputs to each full-adder circuit of an arithmetic logic unit are according to the following Boolean functions:  Xi = AiBi + (s2s1’s0’)’Ai + s2s1s0’Bi  Yi = s0Bi + s1Bi’(s2s1s0’)’  Zi = s2’Ci  Determine the 12 functions of the ALU. | [5] |
| 2.a) | The straight binary subtraction F = A – B produces a correct difference if A ≥ B. What would be the result if A < B? Determine the relationship between the result obtained in F and a borrow in the most significant position. | [3] |
| b) | If *m* = 110110 , *r* = 101101 , *x* = 6 and *y* = 6; using the Booth’s multiplication algorithm determine the initial value of A , S and P. Show all the steps of Booth’s algorithm to find the final value of P. | [5] |
| c) | Deign an arithmetic circuit with two selection variables S1 and S0, that generates the following arithmetic operations. Draw the logic diagram of one typical stage.   |  |  |  |  | | --- | --- | --- | --- | | S1 | S0 | Cin = 0 | Cin = 1 | | 0 | 0 | F = A | F = A + 1 | | 0 | 1 | F = A – B – 1 | F = A – B | | 1 | 0 | F = B – A – 1 | F = B – A | | 1 | 1 | F = A + B | F = A + B +1 | | [6] |
| 3.a) | Draw the block diagram of an 8-bit ALU with a 4-bit status register. The four status bits are symbolized by C, S, Z and V. | [2] |
| b) | Draw the LDA and OUT routines of SAP-1 and also their fetch and execution timing diagram. | [6] |
| c) | Describe the SAP-1 architecture. | [6] |
| 4.a) | What is mnemonics? Explain with example. | [2] |
| b) | Write the status of the **Ring Counter** for each of the following states in SAP-1:   1. Address state 2. Increment state 3. Memory state | [3] |
| c) | How much time delay does this SAP -2 subroutine produce?  MVI A,0AH  LOOP1: MVI B,64H  LOOP2: MVI C,47H  LOOP3: DCR C  JNZ LOOP3  DCR B  JNZ LOOP2  DCR A  JNZ LOOP1  RET | [4] |
| d) | The traffic lights on a main road show green for 50 s, yellow for 6 s, and red for 30 s. Bits 1, 2 and 3 of port 4 of SAP-2 are the control inputs to peripheral equipment that runs these traffic lights. Write a program in mnemonics for SAP-2 that produces time delays of 50, 6 and 30 s for the traffic lights. | [5] |
| 5. | **Figure 1:** control state diagram for question no. 5  z = 0    x = 0 x = 1 y = 1 x=1,y=0    y = 0      z = 1  z=0,y=1  The state diagram of a control unit is shown in Figure 1. It has eight states and three inputs x, y and z. |  |
| a) | Design the control using eight D flip-flops. | [4] |
| b) | Design the control using three J-K flip-flops and a 3×8 decoder. | [5] |
| c) | Design the control using a PLA. | [5] |
| 6.a) | Translate the following program into SAP-1 machine language.   |  |  | | --- | --- | | Address | Instruction | | 0H | LDA 9H | | 1H | ADD AH | | 2H | ADD BH | | 3H | SUB CH | | 4H | OUT | | 5H | HLT | | 9H | 01H | | AH | 02H | | BH | 03H | | CH | 04H | | [3] |
| b) | Serial data is sometimes called a serial data stream because bits flow one after another. In SAP-2 a serial data stream drives bit 7 of port 2 at a rate of approximately 600 bits per second. Write a program that inputs an 8-bit character in a serial data stream and stores it in memory location 2100H. | [5] |
| c) | Implement a macrooperation to count the number of 1’s presently stored in processor register *R1* and sets processor register *R2* to that number. For example, if *R1* = 00110101, the microprogram routine counts the four 1’s stored in the register and sets register *R2* to the binary number 100. Your implementation must contain the following steps:   1. Flowchart 2. Symbolic microprogram to count the number of 1’s in *R1* 3. Binary microprogram to count the number of 1’s in *R1* | [6] |
| 7.a) | Design a combinational circuit using a ROM. The circuit accepts a 3-bit number and generates an output binary number equal to the square of the input number. | [4] |
| b) | Design a hard-wired control to implement the addition and subtraction of two fixed-point binary numbers represented in sign magnitude form. Your design must include the following steps: |  |
|  | 1. Equipment Configuration | [1] |
|  | 1. Derivation of the Algorithm | [1] |
|  | 1. Flowchart | [2] |
|  | 1. Control state diagram and Sequence of microoperations | [4] |
|  | 1. Design of Hard-wired Control | [2] |
|  | You must use an ALU that has the following function table:   |  |  |  |  |  | | --- | --- | --- | --- | --- | | S2 | S1 | S0 | Cin | Output | | 0 | 0 | 1 | 0 | F = A + B | | 0 | 1 | 0 | 1 | F = A - B | | 1 | 1 | 1 | 0 | F = A’ | | 0 | 0 | 0 | 1 | F = A + 1 | |  |